Claims

[c1] What is claimed is:

1.Dynamic random access memory (DRAM) circuitry comprising:

a DRAM cell having a first end connected to a bit line and a second end connected to a plate line; and

a sensing amplifier electrically connected to the DRAM cell for refreshing the DRAM cell and reading data from the DRAM cell;

wherein the sensing amplifier is capable of changing a potential of the bit line and a potential of the plate line to write data into the DRAM cell.

[c2] 2.The DRAM circuitry of claim 1 wherein the plate line is floating because the plate line is disconnected from a power supply.

[c3] 3.The DRAM circuitry of claim 2 further comprising a voltage equalizer electrically connected to both the bit line and the plate line for equalizing the potential of the bit line and the potential of the plate line before reading the data within the DRAM cell.

[c4] 4.The DRAM circuitry of claim 1 further comprising a bit line isolation for isolating different bit lines and limiting voltages of the bit lines.

[c5] 5.The DRAM circuitry of claim 1 wherein the DRAM cell further comprises a third end connected to a word line, and the word line is turned on when the DRAM cell is to be refreshed or the data within the DRAM cell is to be read.

[c6] 6.The DRAM circuitry of claim 5 wherein the DRAM cell comprises a transistor and a capacitor, the third end of the DRAM cell is a gate of the transistor.

[c7] 7.Dynamic random access memory (DRAM) circuitry comprising:

a plurality of DRAM cells each having a first end connected to a bit line, a second end connected to a plate line and a third end connected to a word line;

a sensing amplifier electrically connected to the DRAM cell for refreshing the DRAM cell and reading data from the DRAM cell; and

a bit line isolation for isolating different bit lines and limiting voltages of the bit lines;

wherein the sensing amplifier is capable of changing a potential of the bit line

and a potential of the plate line to write data into the DRAM cell.